Intel® 31154 133 MHz PCI Bridge

Specification Update

December 2005

Document Number: 300826-009US

Contents

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Revision History

Date	Version	Description
October 2005	009	• Added Errata 14 • Added Specification Change 2 • Added Specification Clarification 3 • Added Documentation Change 5; updated paging references
April 2005	008	• Updated Markings Table 1 • Updated Specification Clarifications table • Added Erratum 11 through 13 • Added Documentation Change 4
November 2004	007	• Added A3 Stepping information throughout the document. • Added Errata 10 • Added Documentation Change 3 • Updated Erratum 4, 5, 6, 7, 8 status to Fixed (due to A3 stepping) • Updated Marking Identification Information Section
July, 2004	006	Added Errata 9
June, 2004	005	Added Errata 8 Specification Change 1, and Documentation Change 2.
June, 2004	004	Added Specification Clarification and Documentation Changes information
April, 2004	003	• Revised Errata 3. • Added Errata 4. through Errata 7.
February 2004	002	• Added new A2 stepping to “Errata” table on page 8. • Added Errata 3, “Several Flops in the JTAG/GPIO circuitry are not asynchronously cleared during reset” on page 11. • Added Specification Clarification 1, “GPIO Pin Connections for Mixed 3V and 5V Implementations” on page 18. • Minor edits throughout.
January 2004	001	First release of this document. Documented two erratum.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Related Documents

Title	Order
Intel® 31154 133 MHz PCI Bridge Datasheet	278821
Intel® 31154 133 MHz PCI Bridge Masquerade Application Note	278807
Intel® 31154 133 MHz PCI Bridge Design-In Considerations with IBM PCI-X to PCI-X Bridge Application Note*	278806
Intel® 31154 133 MHz PCI Bridge Developer's Manual	278848
Intel® 31154 133 MHz PCI Bridge Schematics	278839

Nomenclature

Errata are design defects or errors. These may cause the Intel® 31154 133 MHz PCI Bridge's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 31154 133 MHz PCI Bridge product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Plan Fix:	This erratum may be fixed in a future stepping of the product.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings		Page	Status	Errata
	A2	A3			
1	x	x	11	No Fix	Split Transaction Commitment Limit Register Mechanism Does Not Operate as Implied in the PCI-X Specification
2	x	x	11	No Fix	The PCI Bus Hold Time Requirement of 0 ns Hold Time Is Not Met in PCI33 Mode
3.	x	x	11	No Fix	Several Flops in the JTAG/GPIO circuitry are not asynchronously cleared during reset
4.	x		12	Fixed	PCI-X to PCI Memory Read DWORD near a 1MB boundary may cause the system to hang
5.	x		12	Fixed	PCI-X to PCI Memory Read Block across 1MB boundary may cause data corruption
6.	x		13	Fixed	PCI-X to PCI Memory Read with 4 KByte count and unaligned starting address may result in a system hang
7.	x		13	Fixed	The 31154 Bridge may violate PCI ordering rules in some operating modes
8.	x		14	Fixed	PCI-to-PCI read flow through with destination TRDY# stalls may cause data corruption
9.	x	x	14	No Fix	The 31154 Bridge does not support burst I/O read, I/O Write, Config Read or Config Write in PCI mode.
10.	x	x	14	No Fix	Read Flow Through hangs due to disconnect without data at a buffer boundary
11.	x	x	15	No Fix	Primary side P_SERR# is not asserted for a parity error on AD[63:32] during the data phase of a Split Response to a Read request issued by the 31154 Bridge
12.	x	x	15	No Fix	Secondary status bits may be asserted after power on reset
13.	x	x	16	No Fix	X-to-I Memory Read issued as 32-bit, then retried as 64-bit
14.	x	x	16	No Fix	The RCOMP recalibration cycle may cause parity errors or bus hangs

Specification Changes

No.	Page	Specification Changes
1	17	ILI1 parameter is incorrectly listed as 1000uA max.
2	17	Case Temperature Under Bias Temperature Range Change

Specification Clarifications

No.	Steppings		Page	Specification Clarifications
	A2	A3		
1	x	x	18	GPIO Pin Connections for Mixed 3V and 5V Implementations
2	x	x	18	31154 Power Supply Special Considerations
3	x	x	19	PCI Clock Cycle Time of the 31154 output clocks deviate from the PCI-X (Mode 1, Class 1) jitter clock specification

Documentation Changes

No.	Document Revision	Page	Documentation Changes
1	278821	20	Power supply sequencing description incomplete.
2	278821	21	ILI1 parameter is incorrectly listed as 1000uA max.
3	278848	21	Incorrect Bit in PB_STAT - Pre-Boot Status Table
4	278848	21	Split Completion Message indicates the occurrence of a write-data parity error
5	278821	22	Case Temperature Under Bias Temperature Range Change

Identification Information

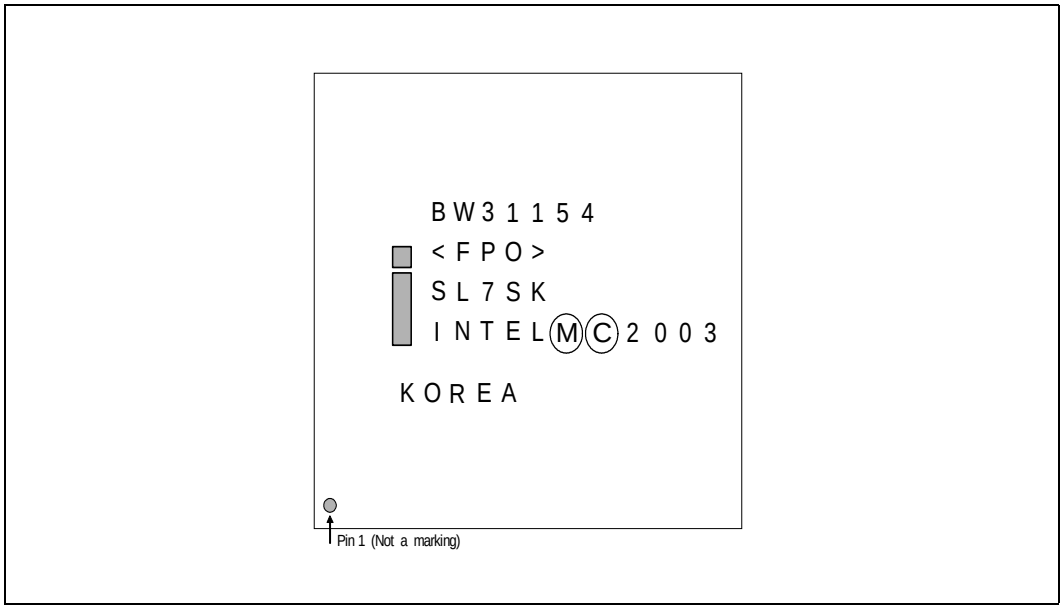
Markings

Table 1. Steppings

Stepping	Revision ID Register Content[a]	Tracking Code	Notes
A2	03h	BW31154	The A2 stepping does not include the SL7SK marking.
A3	07h	BW31154 SL7SK	

a. Steppings for the 31154 Bridge can be identified by reading the contents of the 31154 Bridge Revision ID register at offset 08h in configuration space.

Figure 1. A3 Stepping Identification Markings on 31154 Product



Errata

1. Split Transaction Commitment Limit Register Mechanism Does Not Operate as Implied in the PCI-X Specification

Problem: The Split Transaction Commitment limit register mechanism does not operate as implied in the PCI-X specification[1]. The PCI-X Specification requires that the bridge operate in a fully buffered mode. The Intel® 31154 133 MHz PCI Bridge (hereafter "31154") allows software to write the Split Transaction limit register to allow compatibility with existing software; however, it does behave as if the register is programmed with a value of FFFFh. The bridge forwards all split transactions without regard to the sequence size or the amount of available buffer space.

Implication: This behavior could result in the bridge split completion buffers becoming full while additional split completions are being received. When this situation occurs, the bridge either issues a retry or disconnects on the next ADB, until buffer space is available.

Workaround: None

Status: No Fix

2. The PCI Bus Hold Time Requirement of 0 ns Hold Time Is Not Met in PCI33 Mode

Problem: The bridge does not comply with the PCI33 hold time specification in PCI33 mode The 31154 requires a maximum hold time of 1.66 ns. The PCI-X specification[1] requires a hold time of 0 ns. In all other modes, the PCI requirement of 0 ns is met.

Implication: Hold-time violations may occur when devices installed on the bus do not meet the 2 ns Tval requirement of the PCI specification. Such a violation is most likely to occur in lightly loaded configurations where the other devices attached to the bus do not comply with the 2 ns Tval requirement.

Workaround: None. It is not expected that a device that meets the Tval minimum specification of 2 ns would cause problems.

Status: No Fix

3. Several Flops in the JTAG/GPIO circuitry are not asynchronously cleared during reset

Problem: Several Flops in the JTAG/GPIO circuitry are not asynchronously cleared during reset.

Implication: GPIO[2:0] outputs may come up in an undefined state and will not respond to commands via the device registers. This may also cause the bridge to be non functional if TRST# is asserted then driven high.

Workaround: To initialize the flops for GPIO usage apply 3 or more clock signals to the TCK input to clear the flops. To initialize the flops for JTAG purposes apply 3 or more clock pulses to the TCK input while TRST# is asserted. This may be accomplished in several ways:

1. Connect the SR_CLK input to the TCK input.

   This will provide ~20 clock pulses to the TCK input after P_RST is deasserted and before S_RST is deasserted. A MUX could be used in implementations where both GPIO and JTAG functionality are required.

1. *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0b, July 29, 2002

2. Connect an unused clock output from S_CLK[8:0] to TCK.
   This will clear the flops prior to the deassertion of P_RST.
3. Provide a user supplied clock source to the TCK input.

Status: No Fix.

4. PCI-X to PCI Memory Read DWORD near a 1MB boundary may cause the system to hang

Problem: PCI-X to PCI Memory Read DWORD near a 1MB boundary may cause the system to hang.

Implication: In the following scenario:

A master on the PCI-X bus initiates a Memory Read DWORD through the bridge with a starting address that is not DW aligned and is within the last 4 bytes of a 1MB address boundary. On the PCI side, the bridge initiates the request and disconnects after a single dataphase. The transaction should end at this point, but instead the transaction is then issued a second time with the starting address at the 1MB boundary before being terminated. Back on the PCI-X side, the completion is issued with the correct data for the initial 4-byte request, followed by a second “unexpected” completion. As a result of the second completion, the internal resource counter gets decremented twice, causing the resource checking logic to assume there is no more room on the chip for split transactions. At this point the bridge can no longer process upstream non-posted requests and terminates them with Retry.

Note: The above failure only occurs on a Memory Read DWORD from PCI-X to PCI when the starting address is not DW aligned. A Memory Read DWORD to 0xffffc does not fail, whereas a read to 0xfffff does fail.

Workaround: This issue only affects PCI-X to PCI transactions. PCI to PCI-X, PCI to PCI and PCI-X to PCI-X transactions are not affected. PCI-X to PCI implementations should not attempt to do a Memory Read DWORD that is not DW aligned and is within the last 4 bytes of a 1MB address boundary.

Status: Fixed.

5. PCI-X to PCI Memory Read Block across 1MB boundary may cause data corruption

Problem: PCI-X to PCI Memory Read Block across 1MB boundary may cause data corruption.

Implication: In the following scenario:

A master on the PCI-X bus initiates a Memory Read Block through the bridge with a starting address + byte count that crosses a 1MB boundary. The request is not DWORD aligned and starts less than 3 DWORDS from the 1MB boundary. (ADB). On the PCI side, the bridge initiates the request by setting the low 2 address bits to 00b as required by the PCI specification. The bridge receives data up to the boundary and disconnects, then requests the remainder of the data in a second transaction. On the source bus, the bridge should deliver a small completion up to the 1MB boundary with the BCM bit set. However, the bridge may not set BCM properly or will set BCM but corrupt the byte count for a subsequent completion. In either case the bridge may deliver erroneous data. In some cases other transactions following the bad split completion may contain corrupted data, loose data or contain an incorrect byte count.

Note: For the failure to occur, the starting address and byte count must be set such that request crosses the 1MB boundary. Requests that are DWORD aligned do not fail, nor do requests that do not cross the 1MB boundary (even if they are not aligned).

Workaround: This issue only affects PCI-X to PCI transactions. PCI to PCI-X, PCI to PCI and PCI-X to PCI-X transactions are not affected. PCI-X to PCI implementations that do not cross a 1MB boundary will not experience this issue.

Status: Fixed**.**

6. PCI-X to PCI Memory Read with 4 KByte count and unaligned starting address may result in a system hang

Problem: PCI-X to PCI Memory Read with 4 KByte count and unaligned starting address may result in a system hang.

Implication: The initiator on the PCI-X side issues a Memory Read Block with 4 K request byte count (BC=000h), which the bridge terminates with Split Response. The address in this case is not DWORD aligned (A[1:0] does not = 00b). On the PCI side, the bridge executes the transaction as Memory Read Multiple, but disconnects after only a single dataphase and does not re-issue the transaction. No split completion is returned to the PCI-X bus and the transaction permanently consumes transaction resources and could result in a system hang.

Workaround: Use addresses that are DWORD aligned or any byte count other than 4 K.

Status: Fixed

7. The 31154 Bridge may violate PCI ordering rules in some operating modes

Problem: The 31154 Bridge may violate PCI ordering rules in some operating modes.

Implication: The 31154 Bridge receives and claims a downstream memory write followed by a subsequent memory read request which is immediately enqueued. At the same time, the upstream buffers on the chip are filled with upstream Memory Writes and read completion data. On the destination bus, the memory write is issued in small fragments due to either target disconnect or a low setting of the secondary MLT, and the upstream buffers begin to free up due to delivery of upstream Memory Write data. In between delivery of downstream Memory Write fragments, the bridge issues the subsequent Memory Read, in violation of PCI ordering rules.

Summary of the four failure modes:

1. PCI-to-PCI: A Memory Read transaction may pass a previously enqueued Memory Write.
2. PCI-to-PCI: A Configuration or I/O Read transaction may pass a previously enqueued Memory Write.
3. PCI-to-PCI: A Configuration or I/O Write transaction (including type1 config-to-special cycle) may pass a previously enqueued Memory Write.
4. PCI-X-to-PCI: A Configuration or I/O Write transaction (including type1 config-to-special cycle) may pass a previously enqueued Memory Write.

There is no impact when the bridge is configured in PCI-X to PCI-X mode.

Workaround: Use in PCI-X to PCI-X mode. If the primary bus is PCI and secondary bus is PCI-X, do not use upstream DWORD I/O or type1 config-to-special cycle writes that must be ordered against previously issued Memory Writes.

Status: Fixed.

8. PCI-to-PCI read flow through with destination TRDY# stalls may cause data corruption

Problem: PCI-to-PCI read flow through with destination TRDY# stalls may cause data corruption.

Implication: The scenario is a PCI to PCI Memory Read with flow through enabled (source bus bandwidth is less than or equal to destination bus bandwidth). Requester initiates the read on the source bus, and is retried by the bridge (executed as a delayed transaction). The bridge plays the transaction on the destination bus and starts receiving data from the target. After getting 2-3 cachelines, the transaction is requested again on the source bus, and the bridge enters flow-through. The target device on the destination bus begins to insert target wait-states, and eventually ends the transaction by stalling TRDY# for a number of clocks then signaling disconnect without data at the cacheline boundary. On the source bus, the bridge delivers an extra garbage dataphase beyond what was received on the destination side, causing data corruption.

The affected mode is PCI-to-PCI only. Neither PCI-X-to-PCI-X nor PCI-to-PCI-X modes allow TRDY# stalls on the destination side.

Workaround: In a system that has devices that may terminate transactions in the above manner, the Prefetch Policy registers need to be set so that the target is not given the opportunity to significantly stall TRDY#. For example: If a device can provide 256 bytes in a timely manner, but will delay a request for 384 bytes, the first read and reread factors must not be set higher than 01h (gives an MRM prefetch of 256bytes assuming a 64-byte cacheline size).

Status: Fixed

9. The 31154 Bridge does not support burst I/O read, I/O Write, Config Read or Config Write in PCI mode.

Problem: The 31154 does not support burst I/O read, I/O Write, Config Read or Config Write in PCI mode.

Implication: In conventional PCI mode, it is legal for a requester to attempt a burst I/O Read, I/O Write, Config Read, or Config Write. The 31154 bridge only supports single dataphase Config and I/O transactions. When a master attempts to issue a burst I/O or Config Read, the bridge does not assert STOP# after the first dataphase, resulting in data corruption of all DWORDs beyond the first. For burst I/O Config Writes, the bridge asserts STOP#, but does not de-assert TRDY# on the final dataphase, resulting in loss of data (The second dataphase is dropped by the bridge). Previous PCI bridge implementations have forced single data phase operation in this mode, with a forced disconnect. PCI-X does not permit these modes of operation.

Workaround: X86 processors do not allow this condition to occur. In non X86 systems that do not preclude these burst mode operations, the application should limit the transfer to a single aligned DWORD (32 bit) operation.

Status: No Fix

10. Read Flow Through hangs due to disconnect without data at a buffer boundary

Problem: Read Flow Through hangs due to disconnect without data at a buffer boundary.

Implication: In PCI to PCI mode an upstream read is issued to the bridge and forwarded to the primary bus, using a calculated prefetch size of at least 3 cachelines. On the primary bus, the target claims the request, and delivers data (with intermittent TRDY# slips) up to a 128-byte boundary, then deasserts TRDY# and waits a number of clocks before disconnecting without data. After the 2nd cacheline gets on chip, the bridge enters flow-through and begins delivering data to the initiator. If the time difference between the end of the primary bus read and the end of the secondary bus read is approximately 10 clocks or less, the bridge may hang after the data is delivered.

Workaround: PCI-X to PCI-X and PCI to PCI-X implementations are not subject to this issue. For PCI to PCI systems in which targets might exhibit the above behavior, set all prefetch factors to 000b. This will set the maximum prefetch size to 2 Cachelines (for MRM) and effectively disable read flow-through. There may be a performance impact due to these settings.

Status: No Fix.

11. Primary side P_SERR# is not asserted for a parity error on AD[63:32] during the data phase of a Split Response to a Read request issued by the 31154 Bridge

Problem: Primary side P_SERR# is not asserted for a parity error on AD[63:32] during the data phase of a Split Response to a Read request issued by the 31154 Bridge.

Implication: This behavior does not comply with the PCI-X spec requirements in Version 1.0a, Section 5.4.1.3. However, it will have no impact in the application.

Workaround: Since no valid data is driven onto the upper AD bus during the data phase of a Split Response cycle, there are no negative side effects of not signaling SERR# in this case.

Status: No Fix.

12. Secondary status bits may be asserted after power on reset

Problem: Uninitialized status bits from the Secondary side of the bridge may be reported in configuration Status registers after an initial power on Reset.

Implication: The Secondary Bus Status Registers are latched by S_CLK. Since the internal secondary clock PLL does not come on until P_RST has deasserted, any secondary status reporting latches that powered on in the wrong state will not get cleared until the first secondary bus clock following P_RST. Therefore, the Configuration Space Status Register, which is clocked by P_CLK, may capture un-initialized secondary bus status bits if the next P_CLK (primary Bus CLK) precedes the first S_CLK (Secondary bus clock).

Note: These status bits have no negative effect on chip operation and will not cause error signals but may lead to confusion if read after a subsequent system error. Most systems will reset the bus prior to enumeration and will not experience this issue.

Workaround: Issue a second hardware or software reset to the bridge.

Status: No Fix

13. X-to-I Memory Read issued as 32-bit, then retried as 64-bit

Problem: A 32 bit mem read transaction from PCI-X to PCI may be retried with REQ64# asserted in violation of the PCI specification.

Implication: A memory read with multiple dataphases requested is issued from the PCI-X side across the bridge and played on the PCI-side of the bridge. This read gets some data and is then disconnected by the target. At the same time, a memory read with starting address less than 4DW from the next ADB is enqueued on the PCI-X side and then issued on the PCI immediately after the first read is disconnected. This read is issued the first time with REQ64# deasserted and is retried by the target (delayed transaction). Some time later, the bridge re-issues this read with REQ64# asserted, violating PCI requirements that REQ64# remain the same for every retry.

Note: This can only occur in PCI-X to PCI transactions. This behavior is fairly common in many PCI devices and generally has minimal side effects on overall system performance. In some systems, depending on the setting of the discard timer, a delay may occur before normal system throughput is restored.

Workaround: Limit the PCI-side to 32-bit only in X-to-I configurations.

Status: No Fix

14. The RCOMP recalibration cycle may cause parity errors or bus hangs

Problem: The RCOMP recalibration cycle may cause a parity error or bus hang in applications running at 133 MHz with a case temperature above 55^{o} C.

Implication: The RCOMP recalibration cycle is triggered off the Primary Bus clock and will update the value of the RCOMP register value approximately every 2mS at 133MHz. Depending on the state of the bus and the temperature of the chip, a parity error or bus hang may be generated 3.8uS after the recalibration. Although we have not observed any failures in applications below 133 MHz and case temperatures of less than 55^{o} C, we advise implementing one of the workarounds described below to eliminate any possible exposure to the issue.

Workaround: We have developed two workarounds capable of resolving this issue:

- Strap the TMODE pins to disable the RCOMP recalibration circuitry and load a default value into the RCOMP registers. The workaround is to tie the TMODE0 bit =1 on the module.
- Use the JTAG interface to disable the RCOMP recalibration circuitry and load a custom value into the RCOMP registers. This work around requires a CPLD to be wired to the JTAG control pins and CPLD code capable of invoking JTAG, disabling the RCOMP recalibration and loading a predefined value into the RCOMP register. In applications where the module may be plugged into a PCI 66 slot at extended temperature it is advisable to holdvoltage tolerances within 7% to guarantee PCI timing.

  For applications that are using a CPLD to correct for the request/grant dance interoperability issue with the 82546GB, the CPLD could also be used to implement the JTAG interface and RCOMP work around. Intel will provide reference CPLD code designed to correct for the 82546GB interoperability issue as well as the RCOMP recalibration issue.

Status: No Fix

Specification Changes

1. ILI1 parameter is incorrectly listed as 1000uA max.

Issue: The I_{LI1} parameter for the 31154 Bridge currently states values of 140µA min to 1000µA max. This is now changed to no minimum value and +/-10µA maximum value.

Affected Docs: *31154 133MHz PCI Bridge Datasheet (278821).*

2. Case Temperature Under Bias Temperature Range Change

Issue: The Case Temperature Under Bias has changed for the 31154 Bridge. Table 15 and Table 16 are updated to indicate the updated range.

Section 3.1, Table 15, second row now appears as follows:

Case Temperature Under Bias	0^{o}C to +95^{o}C

Section 3.2, Table 16, last row now appears as follows:

T_C	Case Temperature Under Bias	0	+95	°C

Affected Docs: *31154 133MHz PCI Bridge Datasheet (278821).*

Specification Clarifications

1. GPIO Pin Connections for Mixed 3V and 5V Implementations

Issue: In order to provide maximum functionality in mixed 3V and 5V implementations, GPIO[2:0] pins are connected to P_VIO and GPIO[7:3] pins are connected to S_VIO.

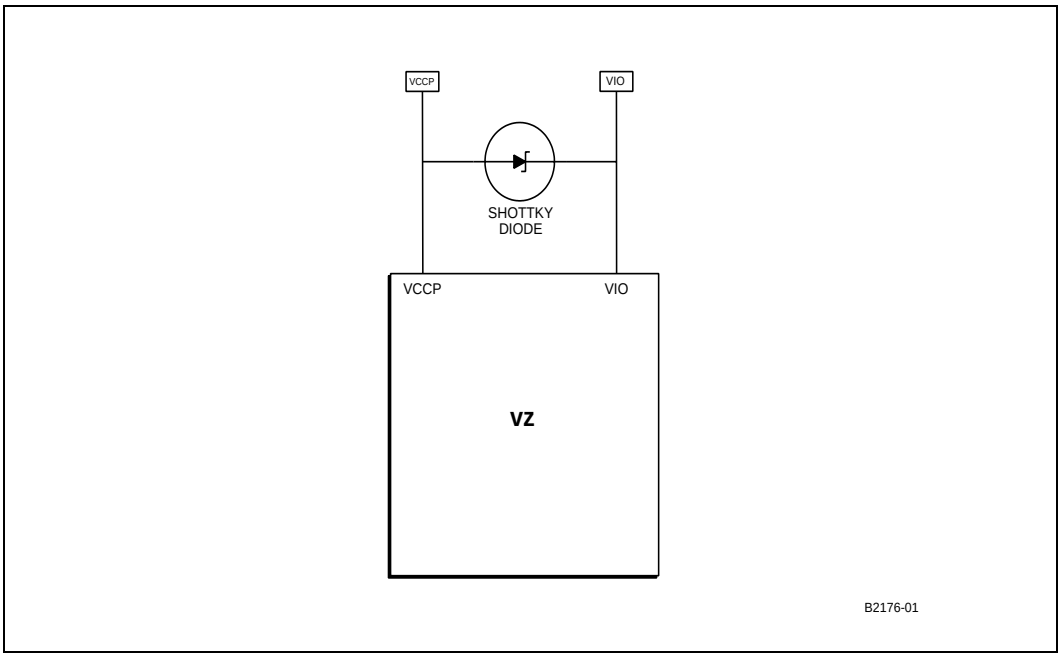
Mixed-voltage designs must use the appropriate GPIO[2:0] or GPIO[7:3] pins.

2. 31154 Power Supply Special Considerations

If either P_VIO or S_VIO is not connected to the same power supply as Vccp, the user must perform one of the following steps:

- Ensure that the P_VIO or S_VIO power comes up before or simultaneously with Vccp and ensure that the P_VIO or S_VIO power goes down after or simultaneously with Vccp.
- Install a Shottky diode, as shown in Figure 1, between VCCP and the VIO pin/pins (as appropriate). The diode should be sized appropriately for the system's power environment. **(Recommended)**
- Connect a 25Ohm current limit resistor in series with the P_VIO and S_VIO supply. P_VIO and S_VIO can never be at a lower voltage than VCCP except in the case of a 25Ohm current limiting resistor in series with the P_VIO and S_VIO supply.

Figure 1. Installing a Shottky Diode



3. PCI Clock Cycle Time of the 31154 output clocks deviate from the PCI-X (Mode 1, Class 1) jitter clock specification

The 31154 generates the PCI-X 133 MHz clock with a nominal frequency of 133 MHz (clock cycle time of 7.5 ns). After considering the clock jitter, clock cycle time (minimum clock period) observed at the pin may be marginally less than 7.5 ns. The PCI-X Class 1 jitter clock specification in Mode 1 requires the clock cycle time to be 7.5 ns with jitter consideration. Clock cycle time deviation may also exists on clocks generated on PCI-X at 100/66 MHz and PCI at 66/33 MHz.

There is no workaround to adjust the clock cycle time of the PCI-X clocks. However, the routing guidelines for the 31154 output clock signals take into consideration the effect of the jitter on the clock cycle time.

Documentation Changes

1. Power supply sequencing description incomplete.

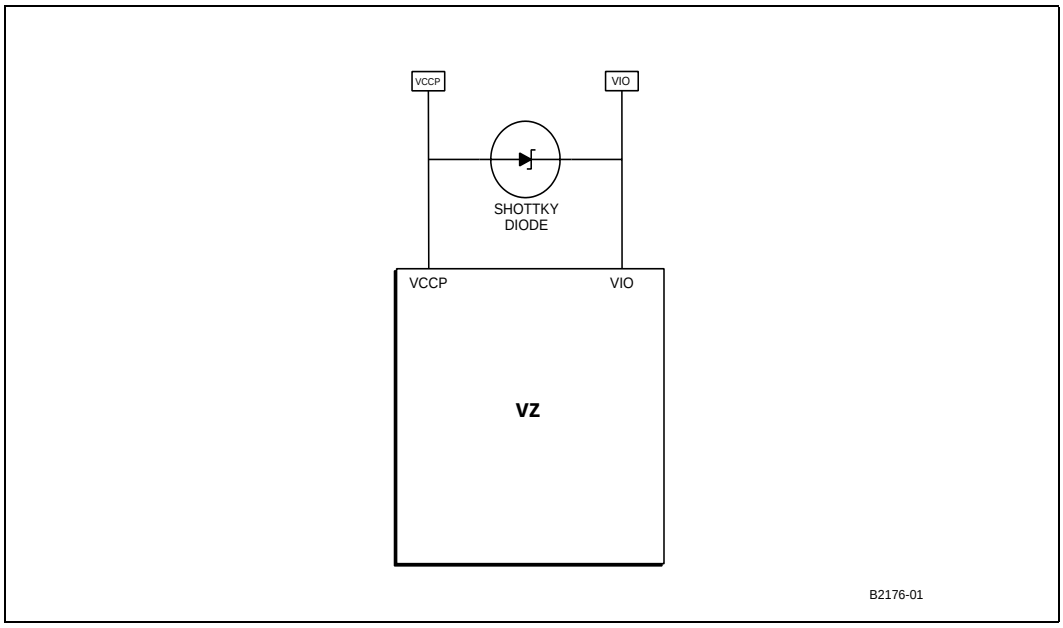
Issue: The description for Section 3.4 does not fully describe the powering sequence for the 31154 Bridge. It should appear as follows:

3.4 Power Supply Special Considerations

If either P_VIO or S_VIO is not connected to the same power supply as Vccp, the user must perform one of the following steps:

- Ensure that the P_VIO or S_VIO power comes up before or simultaneously with Vccp and ensure that the P_VIO or S_VIO power goes down after or simultaneously with Vccp.
- Install a Shottky diode, as shown in Figure 2, between VCCP and the VIO pin/pins (as appropriate). The diode should be sized appropriately for the system's power environment. **(Recommended)**
- Connect a 25Ohm current limit resistor in series with the P_VIO and S_VIO supply. P_VIO and S_VIO can never be at a lower voltage than VCCP except in the case of a 25Ohm current limiting resistor in series with the P_VIO and S_VIO supply.

Figure 2. Installing a Shottky Diode



Affected Docs: *31154 133MHz PCI Bridge Datasheet (278821).*

2. ILI1 parameter is incorrectly listed as 1000uA max.

Issue: In Section 3.7.2, the I_{LI1} parameter (first row in Table 20) is listed as 140µA min to 1000µA max. This is now changed to no minimum value and +/-10µA maximum value. The first row of Table 20 now appears as follows:

Symbol	Parameter	Min	Max	Units
I_{LI1}	Input Leakage Current for each signal except TCK, TMS, TRST#, TDI		±10	µA

Affected Docs: *31154 133MHz PCI Bridge Datasheet (278821).*

3. Incorrect Bit in PB_STAT - Pre-Boot Status Table

Issue: In Section 5.2.12, Offset 56H: PB_STAT - Pre-Boot Status, Bit 07 is documented incorrectly. The bit should be 0b, not 1b.

The table row now appears as follows:

07	0b	Secondary 64-Bit Extension Enabled: Indicates whether the secondary bus 64-bit extensions are enabled. 0b = The secondary bus 64-bit extension are enabled. The 31154 Bridge always enables its secondary bus 64-bit extensions.

Affected Docs: 31154 133MHz PCI Bridge Developer's Manual (278848)

4. Split Completion Message indicates the occurrence of a write-data parity error

Issue: In Section 3.13.3.3 between the second and third paragraph, text should be added as follows:

If the Split Completion Message indicates the occurrence of a write-data parity error (i.e., PCI-X Bridge class and Write Data Parity Error index), the bridge asserts PERR# and sets the appropriate bits in the Status register when the transaction completes on the conventional interface. The 31154 Bridge exhibits this behavior for both PCI-X Bridge Class and Completer Class transactions.

For all other cases in which a non-posted write transaction completes with a Split Completion Message, the bridge terminates the transaction on the conventional interface with Target-Abort.

Affected Docs: 31154 133MHz PCI Bridge Developer's Manual (278848)

5. Case Temperature Under Bias Temperature Range Change

Issue: The Case Temperature Under Bias has changed for the 31154 Bridge. Table 15 and Table 16 are updated to indicate the updated range.

Section 3.1, Table 15, second row now appears as follows:

Case Temperature Under Bias	0^{o}C to $+95^{o}$C

Section 3.2, Table 16, last row now appears as follows:

T_C	Case Temperature Under Bias	0	+95	°C

Affected Docs: *31154 133MHz PCI Bridge Datasheet (278821).*